AMENDMENTS TO THE SPECIFICATION

Please replace paragraphs **[0036], [0038],** and **[0052]** of the specification with the following amended paragraphs.

[0036] In addition to the ability to save data in a manner that appears instantaneous to a user, controller 6 can also revert back to the previously saved state in similar fashion. Specifically, upon receiving a restore command, controller 6 can simply disregard the ~~date~~ data written to secondary virtual storage 10B, thereby reverting to the data stored by primary virtual storage 10A. In this manner, controller 6 can quickly revert to using data stored prior to a time T_0.

[0038] FIG. 2 illustrates an example controller 6 implemented as a single printed circuit board that may be embedded within a host computing device. In this embodiment, controller 6 may include first interface 16, second interface 18, control unit 20, embedded memory 22 and bus interface 24. First interface 16 and second interface 18 provide mechanisms for coupling controller 6 between processor 4 and storage system 8, respectively. Specifically, control unit 20 receives storage access commands from processor 4 via interconnect 12 and first interface 16. In addition, control unit 20 manages and accesses storage system 8 via interconnect 14 and second interface ~~16~~ 18. Although illustrated as implemented on a printed circuit board, controller 6 may be embedded within a mother board along with processor 4, within storage system 8, or within other components of system 2 disposed between processor 4 and storage system 8.

[0052] FIG. 6B illustrates the same logical storage volumes 52A at ~~time~~ a new time T_0 after controller 6 has performed a save operation, thereby reallocating virtual storage 10. In particular primary virtual storage 10A comprises a substantial portion of logical storage volume 52A, but has been reallocated to include portions of logical storage volume 52B.